AMENDMENT TO THE SPECIFICATION

The paragraph commencing at page 2, line 2 is amended as follows:

During manufacture of a protection transistor, an interlayer contact is established between the drain and the gate region by forming a contact hole (throughhole) in the gate insulator using a mask so that part of the gate region is exposed and depositing metal in the contact hole when the drain region is completed. Alternatively, ~~a contact hole is formed~~ after a gate and a drain region ~~and~~ are formed, a contact hole is provided therebetween. ~~The~~ Then, the gate and drain regions are connected through the contact hole when a transparent conductive film is deposited simultaneously with the deposition of the transparent conductive film for pixel electrodes.

The paragraph commencing at page 6, line 6 is amended as follows:

In Figs. 2 and 3, a representative surge protection transistor 14 is shown fabricated on a common glass substrate 20 on which the gate 21 of the transistor is embedded in a gate insulator 22. On the gate insulator 22 is a semiconductor island 23 of amorphous silicon. The source electrode 24 and the drain electrode 25 of the transistor are formed on the opposite sides of the island 23 so that they are separated by a channel with a length "Lch", which forms a channel capacitance "Cch" with the gate 21. Source 24 and the gate 21 overlap with each other by a length "Lgs" to form a gate-source capacitance "Cgs" and the drain 25 and the gate 21 overlap with each other by a length "Lgd" to form a gate-drain capacitance "Cgd". For a gate width Wg of 24 micrometers, each of the overlapping lengths Lgs and Lgd ~~are~~ is equal to 24 micrometers and the channel length Lch is 6 micrometers. Therefore, the capacitances Cgs and Cgd are equal to each other and each of these capacitances is much greater than the channel capacitance Cch.